

complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values.

7. (Amended) An output buffer, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having

predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder having a data mask register, the data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal, the data coder further including a data output register coupled to the data mask register and having the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal;
a second switch coupled between a second voltage node and the data output terminal; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the data output signal has a first logic level responsive to one of the data read output signals having a first predetermined logic level, the data output signal has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data output terminal has the relatively high impedance

responsive to both of the read output signals having other than the first and second predetermined logic levels, respectively.

8. (Amended) An output buffer, comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register generating an output signal a predetermined period after receipt of the DQM signal, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal;

a data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register, the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values.

17. (Amended) A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

23. (Amended) A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit, line to a corresponding input data signal and a complimentary input data signal and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined

values when an active data mask control signal is applied to the data mask control terminal, the data coder having a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further including a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal, the data coder further having a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the output data bit;
a second switch coupled between a second voltage node and the output data bit;

and

 a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the output data bit has a first logic level responsive to one of the data read output signals having a first predetermined logic level, the output data bit has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data bit line has the relatively high impedance responsive to

both of the read output signals having other than the first and second predetermined logic levels, respectively.

24. (Amended) A computer system, comprising:

a processor having a processor data bus, address bus, and control bus;

an input device coupled to the processor;

an output device coupled to the processor;

a memory controller coupled to the processor; and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller, the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output

signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

30. (Amended) A computer system, comprising:

a processor having a processor data bus, address bus, and control bus;

an input device coupled to the processor;

an output device coupled to the processor;

a memory controller coupled to the processor; and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller, the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder having a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further including a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal, the data coder further having a data

output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

 a first switch coupled between a first voltage node and the output data bit;

 a second switch coupled between a second voltage node and the output data bit;

and

 a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the output data bit has a first logic level responsive to one of the data read output signals having a first predetermined logic level, output data bit has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data bit line has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels.

31. (Amended) A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

 an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

 a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register generating an output signal a predetermined period after receipt of the DQM signal, the data mask register further having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal; and

a data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register, the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values.

40. (Amended) An output buffer, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder having a data mask register, the data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register having a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal, the data coder further including a data output register coupled to the data mask register and having the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values, the output stage comprising:

 a first switch coupled between a first voltage node and the data output terminal;
 a second switch coupled between a second voltage node and the data output terminal; and

 a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second

switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level.

47. (Amended) A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder having a data mask register including the data mask control terminal, the data mask

register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active, the data mask register further including a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal, the data coder further having a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

 a first switch coupled between a first voltage node and the output data bit;
 a second switch coupled between a second voltage node and the output data bit;

and

 a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level.